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FREQUENCY DOUBLERS WITH GaAs FET'S

Christen Rauscher
Naval Research Laboratory, Washington, DC 20375

A comprehensive study is presented of single-gate GaAs FET frequency doublers, including self-oscillating doublers, focusing specifically on their applicability to mm-wave power generation. Large-signal simulations are used to identify critical design aspects, with three experimental circuits substantiating the assumptions and predictions.

Introduction

GaAs FETs are well recognized for their capabilities in achieving high efficiency and wideband tunability in microwave oscillators. A unified treatment of fundamental frequency oscillator design has been reported[1]. The present investigation focuses on utilizing the quadratic-type nonlinearities in GaAs FETs to perform frequency doubling. The intent is to extend the use of FETs in RF sources up into the frequency ranges where fundamental frequency oscillation becomes impractical, either due to lack of device gain or due to tuning considerations. What makes the GaAs FET appear attractive as a multiplier are characteristics such as conversion gain, broadband operation, and isolation between input and output. With increasing frequencies of operation these desirable characteristics naturally degrade. They also become more and more interdependent as isolation deteriorates, thereby requiring performance tradeoffs to be made. Based on extensive large-signal simulations, experimental verifications of selected cases, as well as experimental results reported by previous authors[2,3,4], the study outlined in this paper identifies the critical factors in GaAs FET doubler operation and discusses design options.

With reference to a circuit-type quasistatic GaAs FET model of conventional topology, either the nonlinear input capacitance, the nonlinear intrinsic drain-source resistance, and/or the nonlinear transconductance could be utilized, in principle, to provide frequency multiplication. According to large-signal simulations performed earlier[5], the first two alternatives appear rather unattractive due to associated transistor parasitic losses. Supported by experimental results[4], the preferred mode of operation involves modulating the transconductance in the vicinity of pinch-off. This case is studied here.

The doubler configuration most commonly referred to utilizes the transistor in a common source configuration (Fig. 1). It has been observed experimentally[2,3] that conversion efficiency is a strong function of the output terminating impedance Z_{TL} at the fundamental frequency f_0. The simulations and experiments discussed below link this observation to transistor-internal parasitic feedback effects. The logical extension is to supply external feedback at f_0 and/or $2f_0$ to acquire additional design flexibility in trading conversion efficiency against bandwidth and isolation. In the limiting case, provided sufficient gain is available, conversion efficiency goes to infinity, resulting in an oscillator-multiplier.

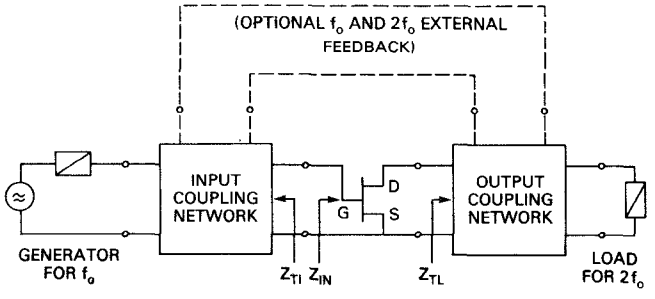

Fig. 1 — GaAs FET frequency doubler

Method of Simulation

For reasons of cost effectiveness and ease of processing the results, a dedicated simulation program was developed. It is based on the so-called harmonic balance approach in which the total circuit is divided into a nonlinear and linear part. In the present context consideration was limited to drain-source nonlinearities. Fixed time-average values were used for all other nonlinearities, as obtained through RF characterization and modeling of device characteristics for a range of bias conditions. Assuming the input at f_0 to be always conjugately matched, the program calculates $2f_0$ output power into an optimally matched second harmonic load for a sequence of discrete f_0 input drive levels. This requires, in effect, a two-dimensional search to be performed versus $2f_0$ load resistance and $2f_0$ load reactance at each drive level. By resorting to the equivalent of a variable transformation an efficient solution was found to this otherwise practically unmanageable optimization task.

Simulation Results and Interpretation

The numerical results given in this context are all based on the Avantek M106 device, possessing a 0.5 μm × 250 μm gate geometry. Small-signal bias conditions were maintained at $V_{DS} = +3.0$ V and $V_{GS} = -1.2$ V, relative to a pinch-off voltage of -1.5 V. With special emphasis on finding out how high up in frequency the FET will perform as an efficient doubler and what the limiting factors are, simulations were performed for fundamental frequencies f_0 spanning K_u-band (WR62). The high end of the band turned out to be more or less the upper practical frequency limit for f_0.

Figure 2 depicts conversion efficiency of a common source doubler (Fig. 1) as a function of second harmonic output power and fundamental frequency reactive load impedance $Z_{TL}(f_0) = j\,50\,\Omega \cdot \tan(\theta)$. The solid curve in Fig. 3 represents the ratio of fundamental frequency power available from the drain-source current generator in a circuit-type device model to the fundamental frequency power incident on the gate-source port of the transistor. This curve was calculated based on fixed time-average values for the nonlinear transconductance and drain-source resistance, thus assuming an entirely linear network. Super-imposed on this curve are conversion efficiency numbers taken from Fig. 2 for second harmonic output power levels of 0 dBm and 8 dBm. The points are represented by the small circles and squares, respectively. All values are normalized at $\theta = 143.5°$, which corresponds to a series resonance at the intrinsic drain-source terminals of the transistor.

The main point of interest here is the strong correlation between the small-signal curve and the large-signal points in Fig. 3. What this demonstrates, in effect, is that the large variations in efficiencies versus f_0 load are not so much the consequence of nonlinear device-circuit interaction, but rather due to transistor internal parasitic feedback. The most rapid changes occur when positive feedback switches to negative feedback as the intrinsic transistor output goes through parallel resonance with correspondingly high voltage swings. This particular transistor is potentially unstable around $f_0 = 15$ GHz, thereby allowing conversion gain to go to infinity for a narrow range of f_0 loads. It is important to remember, however, that increasing conversion gain by appropriate f_0 loading simultaneously increases circuit Q and decreases bandwidth. As mentioned above, additional design flexibility may be obtained by employing external feedback, with its main application being oscillator-multipliers. It is also worth noting that despite the large variations in the curves in Fig. 2 and in the corresponding trajectories in the I_{DS}-V_{DS}-plane (not shown here), the *maximum* achievable second harmonic output power appears to be essentially invariant.

Parasitic feedback effects are equally significant at the second harmonic frequency. This is illustrated by the lower three curves in Fig. 4 which show large-signal conversion efficiency as a function of frequency and second harmonic input termination reactance $Z_{TI}(2f_0) = jX_{TI}(2f_0)$. The simulations show that the pronounced dips are largely due to $2f_0$ signal fed back to the output via the input and interfering destructively at the output. The three upper curves indicate doubler performance with $2f_0$ *external* feedback applied to cancel the destructive interaction. This assumes that the transistor has enough gain, as is the case here, to actually do so.

Experiments

Prior to performing the large-signal simulations a breadboard oscillator-doubler circuit was built to gain some initial experience. The circuit is depicted in Fig. 5 and uses four individual Avantek M110 devices in a balanced configuration. The design employs two fundamental frequency oscillators of the type described in[1], operating push-pull, and a balanced pair of common source doubler transistors with intrinsic drain-source ports series resonated at the fundamental frequency. The second harmonic is probe-coupled to back-shorted Ka-band (WR 28) waveguide.

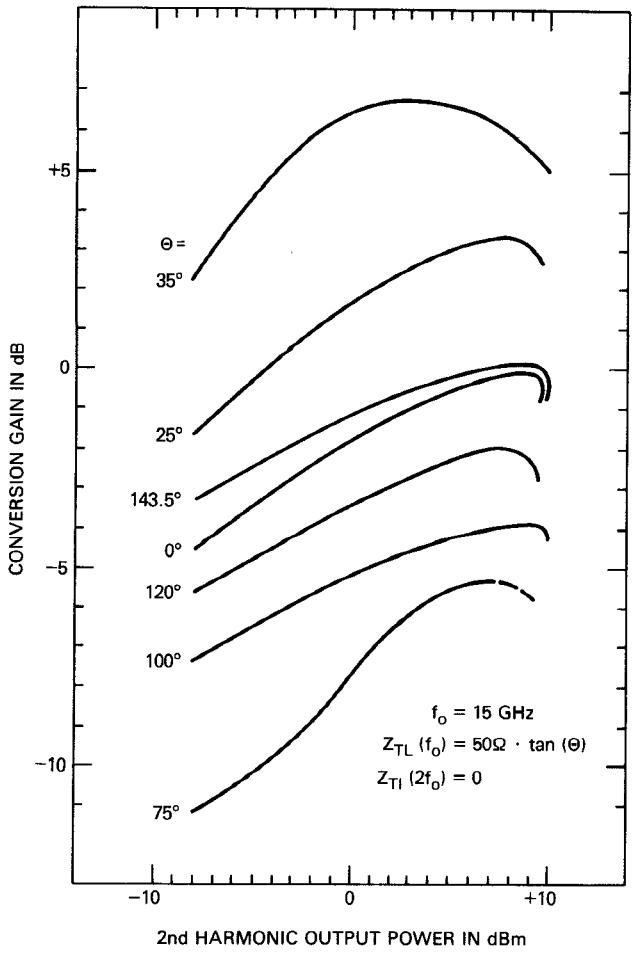

Fig. 2 — Conversion gain as a function of f_0 load reactance and $2f_0$ output power

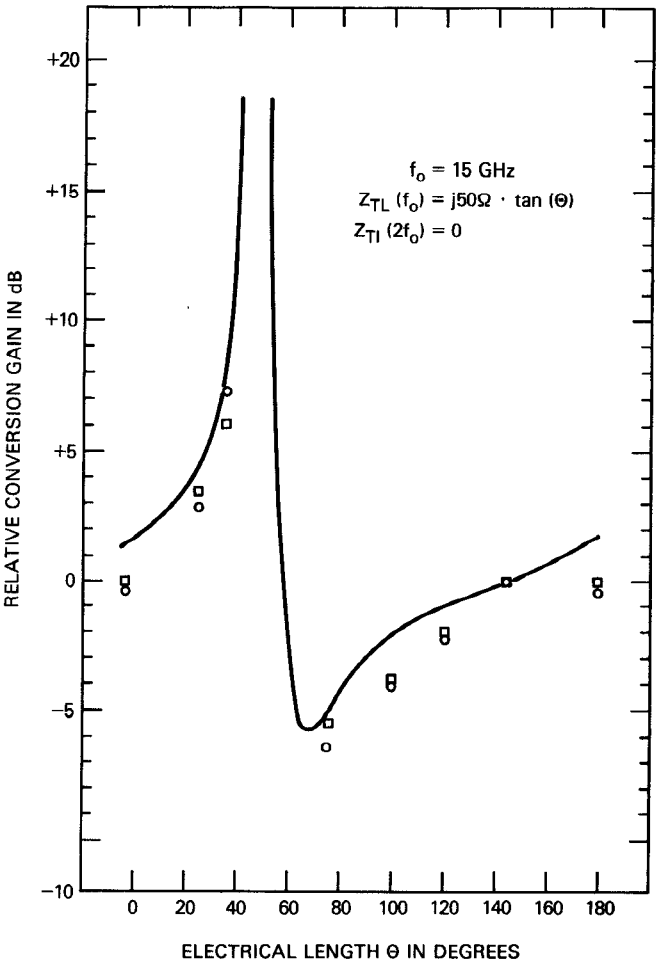

Fig. 3 — Effect of f_0 output termination on conversion gain

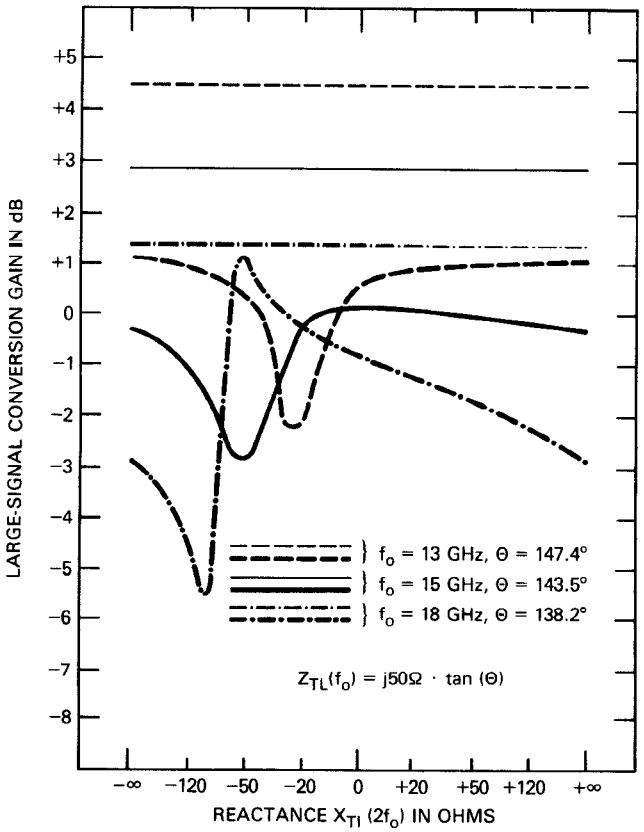

Fig. 4 — Effect of $2f_0$ input termination on conversion gain for series-resonated output at f_0

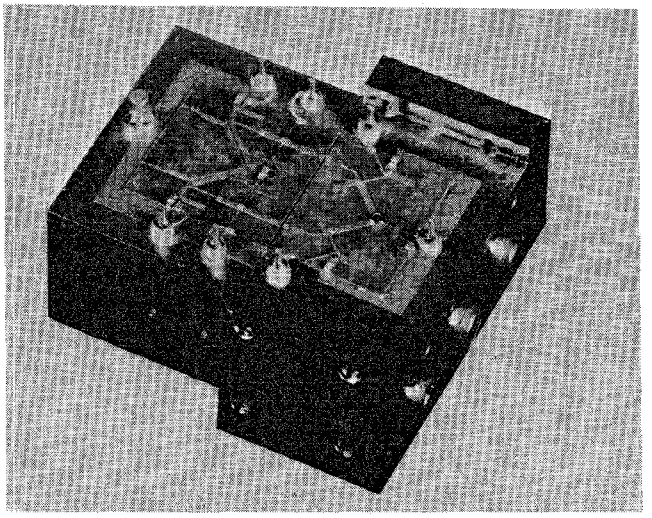

Fig. 5 — Balanced four transistor oscillator-doubler with 12.9 dBm output at 35.6 GHz

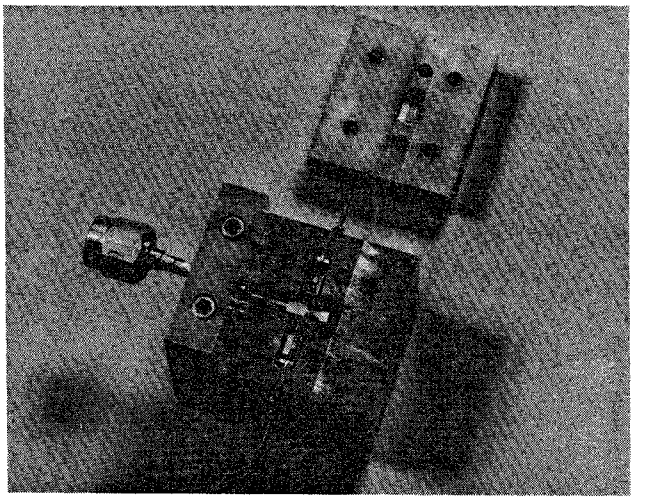

Fig. 6 — Single transistor 15-to-30 GHz frequency doubler

The push-pull oscillator was measured separately and yielded at each of its two ports 14.2 dBm of output power at 17.8 GHz with 16.5 percent efficiency. As the efficiency was lower than previously obtained[1], another single ended oscillator was built, providing an efficiency of 21 percent at 17.3 GHz. It was hence concluded that a major portion of the discrepancy was a consequence of attempting to balance a circuit containing two discrete devices with insufficiently matched characteristics. The complete oscillator-doubler circuit gave 12.9 dBm at 35.6 GHz with an overall DC-to-RF efficiency of 1.75 percent. Although no simulations were carried out for the M110 device, this performance is consistent with data obtained for the M106 device, assuming the combining efficiency at the second harmonic to be comparable to that experienced for the fundamental frequency oscillator devices.

To avoid problems with combining efficiency, the two subsequent experiments involved only single FET circuits using the Avantek M106 devices. Figure 6 shows a 15-to-30 GHz doubler circuit with probe-coupled waveguide output. In order to compensate for unavoidable inaccuracies in assessing parasitics at 30 GHz, especially bondwire parasitics, it was necessary to provide some fine-tuning of input and output circuits. As demonstrated in Fig. 7, the agreement between experiment and prediction is good. Further verification of predicted doubler characteristics was furnished by an oscillator-multiplier designed to generate 9.1 dBm at 30 GHz with the transistor biased at $V_{GS} = -1.2$ V. The measured performance was 8.8 dBm at 29.34 GHz. Changing bias to $V_{GS} = 0$ V increased output power by 0.8 dB, yielding a DC-to-RF efficiency of 9.7 percent.

Conclusions

The extensive set of large-signal simulation results obtained in this investigation emphasize the significance of device parasitic feedback at fundamental and second harmonic frequencies in determining conversion gain and bandwidth. The measured performances of the various experimental circuits support these findings and also serve to verify the appropriateness of the basic assumption that the device output nonlinearities dominate second harmonic generation. Furthermore, it has been demonstrated that DC-to-RF efficiencies approaching 10 percent are readily achievable at Ka-band with oscillator-multipliers employing commonly available half-micron transistors.

References

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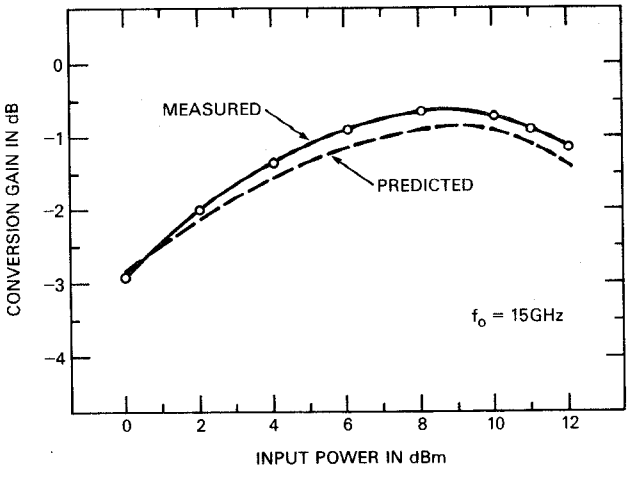

Fig. 7 — Measured and predicted performance of 15-to-30 GHz frequency doubler